

Description

METHOD OF FABRICATING AN INTERCONNECT STRUCTURE HAVING REDUCED INTERNAL STRESS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention generally relates to semiconductor processes, and more particularly to a method of fabricating an interconnect structure having reduced internal stress.

[0003] 2. Description of the Prior Art

[0004] Low-resistance metals such as copper in conjunction with materials with low dielectric constants ("low-k dielectrics") have been used to cope with parasitic capacitance and resistance effects resulting from adjacent interconnect structures fabricated in an integrated circuit chip. As known in the art, circuit performance in the deep sub-micron regime is increasingly a function of the delay time

of electronic signals traveling between the millions of gates and transistors present on the integrated circuit chip.

[0005] Typically, interconnect structures formed on an integrated circuit chip consists of at least about 2 to 8 wiring levels. Fig.1 to Fig.3 are cross-sectional schematic diagrams illustrating a conventional single damascene process. As shown in Fig.1, a lower damascened interconnect 110 is fabricated in a dielectric layer 10. Typically, the lower damascened interconnect 110 consists of a barrier 114 and a copper core 112. After chemical mechanical polishing, a dielectric barrier film 12 such as silicon nitride is deposited over the damascened interconnect 110 and over dielectric layer 10.

[0006] As shown in Fig.2, a chemical vapor deposition (CVD) process is carried out to deposit a low-k dielectric film 14 onto the dielectric barrier film 12. The low-k film deposition process is terminated upon the desired film thickness, for example, 0.45 microns or 0.8 microns, is reached (i.e., one-step deposition). Thereafter, the low-k dielectric film 14 is subjected to a cooling or quenching process in the same CVD reactor (not shown) without breaking the vacuum thereof. After this, another dielectric

barrier film 16 such as silicon nitride is deposited over the low-k dielectric film 14. The dielectric barrier film 16, the low-k dielectric film 14, and the dielectric barrier film 12 constitute a sandwich stack 20.

[0007] As shown in Fig.3, a conventional lithographic process and a dry etching process are carried out to form a recessed trench in the sandwich stack 20. The recessed trench is situated directly above the lower damascened interconnect 110 and exposes a portion of the copper core 112. A barrier layer 124 and a copper layer 122 are then deposited in the recessed trench and then chemical mechanical polished to form the single damascene structure 120.

[0008] However, reliability problems are associated with the above-described prior art structure. For example, such structure is not sufficient to withstand present processing operations including the thermal cycling associated with semiconductor manufacturing. Ordinarily, the semiconductor device is subjected to about 5 to 20 thermal cycles to a temperature of 400–450°C during manufacture. Also, during operation in the field, the device is further subjected to a large number of thermal cycles to a temperature of about 150°C . The reliability testing of completed

IC's commonly includes a "thermal cycle" test in which the part is cycled hundreds of times between a selected low temperature and a selected high temperature.

[0009] One problem associated with the above-described structure is poor adhesion observed at the location of the interface of the upper wire level and bottom wire level. Poor adhesion is due to the high stress level of the material in the layers associated with the interface. This phenomenon is known as peeling. The details of this adhesion problem are not yet sufficiently clear or complete to those skilled in the art. It is believed that the problem of poor adhesion exists due to the high stress level of the material in the layers associated with the interface. Each material in these layers exhibits an internal stress, either tensile or compressive, which can eventually cause curving of the layer superimposed on another layer. By convention, tensile stress has a value greater than zero while compressive stress has a value less than zero. If the stress is particularly high so as to generate forces at the interface, which are greater than the adhesion forces between the layers, peeling occurs.

[0010] Therefore, it would be desirable to provide a method for making an interconnect structure that can provide better

adhesion at the interface of the wire levels as well as a relatively low effective capacitance for the device. It would also be desirable for the interconnect structure to possess a substantially low stress level, i.e., one equal to about zero, thereby providing a stable structure when subjected to thermal cycles at both low temperatures, e.g., room temperature, and at high temperatures, e.g., temperatures above about 150°C .

SUMMARY OF INVENTION

[0011] It is the primary object of the present invention to provide a method for making an interconnect structure that possess a substantially low stress level.

[0012] According to the claimed invention, a method of fabricating an interconnect structure having reduced internal stress is provided. A semiconductor substrate having a base dielectric layer thereon is prepared. A damascened interconnect structure is formed in the base dielectric layer. The damascened interconnect structure is capped with a first dielectric barrier. A first chemical vapor deposition (CVD) process is executed within a CVD reactor to deposit a first low-k dielectric film having a pre-selected thickness onto the first dielectric barrier. Subsequently, a first cooling process is carried out within the CVD reactor

for cooling down the first low- k dielectric film. A second CVD process is performed within the CVD reactor to deposit a second low- k dielectric film having the pre-selected thickness onto the first low- k dielectric film. A second cooling process is carried out within the CVD reactor for cooling down the first and second low- k dielectric films. The first and second low- k dielectric films constitute a low- k film stack having reduced internal stress. The low- k film stack is then capped with a second dielectric barrier.

[0013] From one aspect of the present invention, a copper damascene process is provided. A semiconductor substrate having a base dielectric layer thereon is prepared. A first damascened copper interconnect structure is formed in the base dielectric layer. The first damascened copper interconnect structure is capped with a dielectric barrier; Subsequently, multiple chemical vapor deposition (CVD) cycles within a CVD reactor is carried out to deposit a low- k dielectric film stack on the first dielectric barrier until thickness of the low- k dielectric film stack reaches a desired value, wherein each of the CVD cycles comprises: (1) chemical vapor depositing a low- k dielectric film having a pre-selected thickness; and (2) cooling down the

low-k dielectric film within the CVD reactor. A second damascened copper interconnect structure is formed in the low-k dielectric film stack, such that the first damascened copper interconnect is electrically connected to the second damascened copper interconnect structure.

[0014] Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0016] Fig.1 to Fig.3 are cross-sectional schematic diagrams illustrating a conventional single damascene process;

[0017] Fig.1 to Fig.8 are cross-sectional schematic diagrams illustrating an exemplarily preferred single damascene process in accordance with the present invention method; and

[0018] Fig.9 is a comparison plot showing the internal stress vs.

thickness of the CVD low-k film.

DETAILED DESCRIPTION

[0019] Please refer to Fig.4 to Fig.8. Fig.4 to Fig.8 are cross-sectional schematic diagrams illustrating an exemplarily preferred single damascene process in accordance with the present invention method, wherein like numerals designate similar regions, layers or elements. It is appreciated that the present invention should not be limited to the depicted single damascene process though the single damascene process is taken as an example in this specification for the sake of simplicity. The present invention method may also be applied to other damascene processes such as trench-first, via-first, or partial-via dual damascene processes or the like to achieve the purpose of reducing internal stress of the CVD low-k films. Hereinafter, the term "low-k film" or "low-k dielectric film" refers to a dielectric layer having a dielectric constant that is less than 3.0.

[0020] As shown in Fig.4, a lower damascened interconnect 110 is fabricated in a dielectric layer 10. Likewise, the lower damascened interconnect 110 consists of barrier 114 such as titanium or titanium nitride, and a copper core 112. After chemical mechanical polishing, a dielectric bar-

rier film 12 such as silicon nitride is deposited over the damascened interconnect 110 and over dielectric layer 10 that is substantially coplanar with the exposed surface of the damascened interconnect 110.

[0021] As shown in Fig.5, a first-cycle chemical vapor deposition (CVD) process is carried out to deposit a low-k dielectric film 14a onto the dielectric barrier film 12. The first-cycle CVD process is terminated prior to the desired film thickness is reached. By way of example, assuming that the desired film thickness is 0.45 microns, the preferred thickness of the low-k dielectric film 14a may be about 0.15 microns, but not limited thereto. In another case, the thickness of the low-k dielectric film 14a may be about 0.05~0.2 microns, more preferably 0.1~0.15 microns. After depositing the low-k dielectric film 14a to the first thickness (e.g., 0.15 microns), in the same CVD reactor, the low-k dielectric film 14a is then subjected to a standard cooling process for cooling down to room temperature (i.e., about 25°C). Typically, the cooling process takes place in a separate cooling chamber of the CVD reactor or CVD apparatus known in the art.

[0022] As shown in Fig.6, subsequently, a second-cycle CVD process is carried out to deposit a low-k dielectric film 14b

onto the low-k dielectric film 14a. Still, the second-cycle CVD process is terminated prior to the desired film thickness is reached. In a case that the desired film thickness is 0.45 microns, the preferred thickness of the low-k dielectric film 14b may be about 0.15 microns, but not limited thereto. After depositing the low-k dielectric film 14a to the second thickness (0.15 microns), the low-k dielectric film 14a and the low-k dielectric film 14b are together subjected to a standard cooling process within the CVD reactor for cooling down to room temperature (i.e., about 25°C).

[0023] As shown in Fig.7, a third-cycle CVD process is carried out to deposit a low-k dielectric film 14c onto the low-k dielectric film 14b. The third-cycle CVD process is terminated upon the desired film thickness is reached. In a case that the desired film thickness is 0.45 microns, the preferred thickness of the low-k dielectric film 14c is about 0.15 microns. Again, after depositing the low-k dielectric film 14c to the third thickness (0.15 microns), the low-k dielectric film 14a, 14b, and 14c are together subjected to a standard cooling process within the CVD reactor for cooling down to room temperature. Thereafter, another dielectric barrier film 16 such as silicon nitride is de-

posited to cap the low-k dielectric film 14c. The dielectric barrier film 16, the low-k dielectric films 14a, 14b, and 14c, and the dielectric barrier film 12 constitute a sandwich stack 20.

[0024] As specifically indicated, the combination of the first thickness of the low-k dielectric film 14a, the second thickness of the low-k dielectric film 14b, and the third thickness of the low-k dielectric film 14c is the desired film thickness: 0.45 microns. It is noted that the compositions of each of the three low-k dielectric film 14a, 14b, and 14c are substantially the same, because they are all deposited under the same CVD operation conditions. It is also noteworthy that according to the above-described preferred embodiment the low-k dielectric film 14a went through three-time cooling steps, while the low-k dielectric film 14b went through two-time cooling steps before capped by the dielectric barrier film 16.

[0025] As shown in Fig.8, a conventional lithographic process and a dry etching process are carried out to form a recessed trench in the sandwich stack 20. The recessed trench is situated directly above the lower damascened interconnect 110 and exposes a portion of the copper core 112. A barrier layer 124 and a copper layer 122 are then

deposited in the recessed trench and then chemical mechanical polished to form the single damascene structure 120.

[0026] Though a bit of the throughput may suffer due to the introduction of additional cooling steps, it is still desired to replace the prior art one-step CVD low-k film deposition with the multi-stage CVD low-k film deposition of the present invention because by doing this a significant internal stress reduction of the CVD low-k film can be obtained, thus improving device reliability.

[0027] Fig.9 is a comparison plot showing the internal stress (MPa) vs. thickness (kilo-angstrom) of the CVD low-k film, wherein experimental results regarding both prior art one-step CVD deposition and the multi-stage CVD deposition are demonstrated. As seen in Fig.9, a one-step CVD low-k film with a desired thickness of 0.45 microns (4.5 kilo-angstroms) has an internal stress or residual stress of about 42 MPa. Compared to the prior art one-step CVD low-k film, the present invention multi-stage CVD low-k film with a desired thickness of 0.45 microns has a much lower internal stress of about 15 MPa.

[0028] Those skilled in the art will readily observe that numerous modifications and alterations of the present invention

method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.